a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length;

a contact connected to one of the source and drain diffusion layers; and

a first insulating film, different from silicon oxide, covering the second transistor and not covering the first transistor, the first insulating film having a property that makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

20. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher from a surface of the insulating film.

22. (Amended) The nonvolatile semiconductor memory device according to claim 21, wherein the etching stopper insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher from a surface of the etching stopper insulating film.

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion is respectfully requested.

Claims 1-3, 5, 11-14, and 19-25 are presently active. Claims 1, 20, and 22 have been amended by the present amendment. The changes to the claims were supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, the Examiner rejected Claims 1-3 and 5 under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 4,495,693 to Iwahashi et al. (hereinafter "the '693 patent"), in view of published U.S. Patent Application No. 2001/0002711 A1 to Gonzalez (hereinafter "the '711 application").[2] Further, Claims 11, 14, 19, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '693 and '711 patents, further in view of U.S. Patent No. 4,769,340 to Chang et al. (hereinafter "the '340 patent") and U.S. Patent No. 4,866,003 to Yokoi et al. (hereinafter "the '003 patent"). Finally, Claims 12, 13, and 21-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '693 patent, the '711 application, the '340 patent, and the '003 patent, further in view of U.S. Patent No. 4,467,452 to Saito et al. (hereinafter "the '452 patent") and U.S. Patent No. 5,731,130 to Tseng (hereinafter "the '130 patent").

Amended Claim 1 is directed to a nonvolatile semiconductor memory device including (1) a semiconductor substrate, (2) an element isolation region formed in the substrate, (3) a first transistor formed in a peripheral circuit portion of the substrate, (4) a second transistor formed in a memory cell portion of the substrate, (5) a contact, and (6) a first insulating film, different from silicon oxide, covering the second transistor and not covering the first transistor. Claim 1 has been amended to delete the limitation that the first insulating film is "an etching stopper for the contact to the element isolation region."

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[2]Applicants note that a rejection under 35 U.S.C. § 102(b) over a combination of references is improper. Accordingly, Applicants will assume that Claims 1-3 and 5 are rejected under 35 U.S.C. § 103(a) only.

Regarding the rejection of Claim 1 under 35 U.S.C. § 103, the Office Action states that the '693 patent discloses everything in Claim 1 with the exception of the first insulating film being different from silicon oxide, and relies on the '711 patent to remedy the deficiency.

The '693 patent is directed to a semiconductor memory device having an MOS transistor and a floating-gate-type MOS transistor. Referring to Figure 11ℓ, the Office Action indicates that the '693 patent discloses an insulating film 158 covering a second transistor. However, Applicants submit that the '693 patent fails to disclose that insulating film 158 does not cover a first transistor.[3] Regarding the insulating film 158, the '693 patent discloses:

> In the high temperature heat treatment step, the surfaces of the semiconductor substrate 128, floating gate 122, control gate 124 and gate electrodes 138C and 138D are thermally oxidized to form a third oxide film 158.[4]

Thus, as illustrated in Figure 11ℓ, the '693 patent discloses that the first insulating film covers *all* of the transistors in the '693 device.

The '711 application is directed to an improved storage node junction in a DRAM memory cell. However, Applicants submit that the '711 application fails to disclose a first insulating film covering a second transistor and not covering a first transistor, wherein the first transistor is formed in a *peripheral circuit portion* of the semiconductor substrate, as recited in Claim 1. Note that while Figure 1 of the '711 application shows an insulating film 30 covering multiple transistors, none of the transistors shown in the '711 application

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[3]The Office Action identifies the claimed first transistor as being formed in peripheral circuit 166 and the claimed second transistor as being formed in the memory cell portion 120. See Figure 11ℓ of the '693 patent.

[4]'693 patent, column 11, lines 19-23.

correspond to a transistor formed in a peripheral circuit portion, where the peripheral circuit portion is defined as in Claim 1.[5]

Thus, no matter how the teachings of the '693 patent and '711 application are combined, the combination does not teach or suggest the first insulating film recited in Claim 1. Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 1 (and dependent Claims 2, 3, and 5) should be withdrawn.

Claim 11 is directed to a nonvolatile semiconductor memory device including a semiconductor substrate, a plurality of memory cell transistors, a plurality of peripheral transistors, and an insulating film. Further, Claim 11 recites that the surface of the insulating film is oxidized.

Regarding the rejection of Claim 11 under 35 U.S.C. § 103, Applicants note that none of the cited references discloses that the surface of the insulating film is oxidized, as recited in Claim 11. In particular, note that the insulating film 7 of the '003 patent (cited by the Office Action) is not an etch stop, but an intermediate insulating layer made of silicon oxide insulating film.[6] Further, the silicon nitride film 12 of the '003 patent covers only the top surface of a transistor. Thus, the '003 patent fails to disclose an insulating film covering a side and top of both a plurality of erasable and programmable memory cell transistors and a plurality of peripheral transistors, as recited in Claim 11. Accordingly, Applicants

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[5]Moreover, the Office Action does not assert that the '711 application discloses a first transistor formed in a peripheral circuit. Rather, the '711 application only is asserted by the Office Action to teach an insulating film different from silicon oxide.

[6]See column 3, lines 28-29 of the '003 patent.

respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 11 (and dependent Claim 14) should be withdrawn.

Regarding the rejection of Claim 12, which depends from Claim 11, the Office Action relies on the '452 patent to disclose the claimed thickness of the insulating film. However, Applicants respectfully submit that the '452 patent does not cure the deficiencies of the '693 patent, the '711 application, the '003 patent, and the '340 patent with regard to the claimed insulating film, namely that the surface of the insulating film is oxidized. Thus, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 12 be withdrawn.

Regarding the rejection of Claim 13, which depends from Claim 11, the Office Action relies on the '130 patent to disclose the thickness of the claimed oxidized region of the insulating film. The '130 patent discloses a silicon nitride inter-electrode dielectric film 40 on the surface of the capacitor bottom electrodes. However, Applicants respectfully submit that the '130 patent does not cure the deficiencies of the '693 patent, the '711 application, the '340 patent, and the '003 patent with regard to the claimed insulating film, as discussed above. Thus, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and the rejection of Claim 13 be withdrawn.

Regarding the rejection of Claim 21, Claim 21 recites limitations analogous to the limitations recited in Claim 11. Accordingly for the reasons stated above for the patentability of Claim 11, Applicants respectfully submit that a *prima facie* case of obviousness has not been established and that the rejection of Claim 21 (and dependent Claims 22-25) should be withdrawn.

Thus, it is respectfully submitted that Claim 1 (and dependent Claims 2, 3, and 5), Claim 11 (and dependent Claims 12-14, 19, and 20), and Claim 21 (and dependent Claims

22-25) patentably define over the '693, '003, '452, '130, and '340 patents, and the '711 application.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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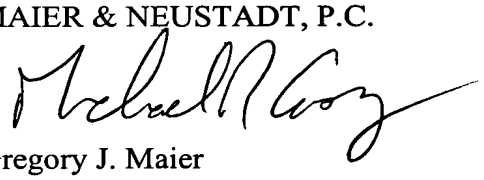

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IN THE CLAIMS

Please amend Claims 1, 20, and 22.

1. (Twice Amended) A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

an element isolation region formed in the semiconductor substrate, the element isolation region isolating a plurality of element regions in the semiconductor substrate;

a first transistor formed in a peripheral circuit portion of the semiconductor substrate, the first transistor including source and drain diffusion layers formed in one of the plurality of element regions and a gate electrode having a first gate length;

a second transistor formed in a memory cell portion of the semiconductor substrate, the second transistor including source and drain diffusion layers formed in another of the plurality of element regions and a gate electrode having a second gate length shorter than the first gate length;

a contact connected to one of the source and drain diffusion layers; and

a first insulating film, different from [a] silicon oxide, covering the second transistor and not covering the first transistor, the first insulating film [being an etching stopper for the contact to the element isolation region and] having a property [which] that makes it difficult for an oxidizing agent to pass therethrough compared with the silicon oxide.

20. (Amended) The nonvolatile semiconductor memory device according to claim 11, wherein the insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher [near] from a surface of the insulating film.

22. (Amended) The nonvolatile semiconductor memory device according to claim 21, wherein the etching stopper insulating film has a concentration gradient in which the hydrogen concentration gradually becomes higher [near] from a surface of the etching stopper insulating film.